This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): In a method of manufacturing a semiconductor device comprising plural adjacent transistor cells provided with a gate electrode and a diffusion layer disposed adjacent to each of opposite end portions of said gate electrode, the method comprising the steps of:

forming a conductive layer on a semiconductor substrate through an insulation film;

patterning said conductive layer to form said gate electrode together with a shielding electrode, wherein said shielding electrode is disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said gate electrode as a continuous line;

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said gate electrode and said shielding electrode as masks to form said diffusion layer; and

insulating said gate electrode in each of said transistor cells,

wherein said diffusion layer forms a diffusion line extending, in a completed device, between said adjacent transistor cells.

Claim 2 (currently amended): In a method of manufacturing a nonvolatile semiconductor memory device provided with a plurality of integrated nonvolatile semiconductor memory cells each comprising: a lower floating gate; a control gate formed on said lower floating gate through an insulation film; a diffusion layer disposed adjacent to each of opposite end portions of said lower floating gate, the method comprising the steps of:

forming a first conductive layer on a semiconductor substrate through an insulation film;

patterning said first conductive layer to form said lower floating gate together with a device isolation shielding electrode, wherein said shielding electrode is formed as a continuous line disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said lower floating gate between plural of said nonvolatile memory cells in a completed device; and

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said lower floating gate and said device isolation shielding electrode as masks to form said diffusion layer,

wherein said diffusion layer forms a diffusion line extending, in the completed device, between adjacent ones of said nonvolatile memory cells.

Claim 3 (original): The method of manufacturing the nonvolatile semiconductor memory device, according to claim 2, wherein: in said step of patterning said first conductive layer to form said lower floating gate together with said device isolation shielding electrode, a first floating gate and a second floating gate extending in parallel with said first floating gate are formed.

Claim 4 (original): The method of manufacturing the nonvolatile semiconductor memory device, according to claim 2, wherein: in said step of injecting said impurity into said semiconductor substrate in a self-align manner with the use of both said lower floating gate and said device isolation shielding electrode as said masks to form said diffusion layer, said diffusion layer is so formed as to cover adjacent ones of said nonvolatile semiconductor memory cells.

Claim 5 (original): The method of manufacturing the nonvolatile semiconductor memory device, according to claim 2, wherein the method further comprises the steps of:

forming a floating gate covering insulation film for covering said lower floating gate, wherein said steps of forming said floating gate covering insulation film follows said step of injecting said impurity into said semiconductor substrate in said self-align manner with the use of both said lower floating gate

and said device isolation shielding electrode as said masks to form said diffusion layer;

forming a second conductive layer for covering said floating gate covering insulation layer;

patterning said second conductive layer to form said control gate extending in a direction substantially perpendicular to a longitudinal direction of each of said lower floating gate and said device isolation shielding electrode; and

patterning said lower floating gate in a self-align manner with the use of said control gate as a mask to have only a portion of said lower floating gate immediately under said control gate remain.

Claim 6 (original): The method of manufacturing the nonvolatile semiconductor memory device, according to claim 5, wherein said step of patterning said second conductive layer is performed by:

covering said second layer with a second conductive layer covering insulation film;

patterning said second conductive layer covering insulation film to form a mask insulation film; and

using said mask insulation film as a mask.

Claim 7 (original): The method of manufacturing the nonvolatile semiconductor memory device, according to claim 6, wherein said step of patterning said lower floating gate is

performed by using both a resist film and said mask insulation film as masks in a self-align manner in a condition in which said device isolation shielding electrode is covered with said resist film.

Claim 8 (original): The method of manufacturing the nonvolatile semiconductor memory device, according to claim 5, wherein the method further comprises the step of forming a third conductive layer by:

covering said lower floating gate with a third conductive layer before said step of forming said floating gate covering insulation film is performed; and

patterning said third conductive layer in a manner such that said third conductive layer is larger in area size than said lower floating gate, so that an upper floating gate is formed.

Claim 9 (original): The method of manufacturing the nonvolatile semiconductor memory device, according to claim 8, wherein: each of said first, second and said third conductive layer is made of polysilicon.

Claim 10 (currently amended): In a method of manufacturing a semiconductor device provided with a gate electrode and a diffusion layer <u>for a drain line and another diffusion layer for a source line</u> disposed adjacent to each of opposite end portions of said gate electrode, the method comprising the steps of:

forming a conductive layer on a semiconductor substrate through an insulation film;

patterning said conductive layer to form said gate electrode together with a shielding electrode, wherein said shielding electrode is formed as a continuous line disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said gate electrode;

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said gate electrode and said shielding electrode as masks to form said diffusion ~~layer~~ layers covering adjacent ones of transistor cells; and

insulating said gate electrode in each of said transistor cells,

wherein said diffusion ~~layer of each of said transistor cells~~ layers are of the same width and form diffusion source and drain lines of equal width extending, in a completed device, between adjacent memory cells.